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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,061	02/11/2002	Donald C. Soltis JR.	10016639-1	6701

7590 10/05/2005

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EXAMINER	
PAN, DANIEL H	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,061	SOLTIS ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/08/05, 07/22/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3* is/are allowed.

6)☒ Claim(s) *4,5 and 7-16* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-16 are presented for examination. Upon further review and consideration. The finality of last office action on 02/22/05 is herein withdrawn. This action supersedes the previous office action. This action includes indication of allowable claim 1, and newly applied art Fetterman et al. (5,627,985), and already applied art Panwar (5,884,070) , Iadonato et al. (5,371,684) and Wang et al. (5,826,055) on the record with additional arguments and comments to allow applicant to respond. Therefore, this is a non-final action.

2. In view of the Appeal Brief filed on 07/22/05 , PROSECUTION IS HEREBY REOPENED. A new ground of rejection which is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 8,15 are rejected under 35 U.S.C. 102(b) as being anticipated by Fetterman et al. (5,627,985).

4. As to claims 8,15, Fetterman taught :

a) aliasing each register identifier of a group of register identifiers (see one of the [EAX] –[EDX] registers in fig.3 in the aliasing table) to two or more registers (see EAX register mapping to corresponding physical register and real register in a single entry of EAX in col.8, lines 41-49) of a register file of the processor; and

b) determining data hazards with the register file by processing one or more of the register identifiers (see the determination of the validity of the speculative result of the corresponding architectural register to the committed real register in col.8, lines 45-49).

The architectural registers are the EAX-EDX (see col.7, lines 10-15).

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (5,826,055) in view of Panwar (5,884,070).

6. As to claim 4, Wang disclosed at least :

a) register file (see register file col.10, lines 1-5),-

b) an execution unit having an array of pipelines for processing instructions (see col.1, lines 45-52) and for writing bypass data in to the register file (see col.10, lines 1-5)',

c) data hazard detection logic for detecting data hazard detection (see col.l, lines 54-54 for background, see col.6, lines 57-67).

7. Wang did not specifically show the aliasing for two or more rows of the register files as claimed. However, Panwar disclosed aliasing of two or more rows in a register file (see fig.1B). See the aliased register f4 and register f5 with f4 ID in fig.1B. See fig.1A for rows of original register file. It would have been obvious to one of ordinary skill in the art to use Panwar in Wang for including the aliasing of the two rows as claimed because the use of Panwar could provide the capability of Wang to accept to different groups of registers in a given reference, therefore reducing the hardware space, and it could be achieved by predefining the aliased register file of Panwar into Wang with modified register pointer so that the aliased rows of register file of Panwar could be recognized by Wang) in order to archive the reduced dependencies control of Wang, and because Wang also suggested the use of aliased register table as a background art (see page 2 , lines 7-9 of cited reference in Wang), and for the above reasons, provided a motivation.

8. As to claim 5, Wang also included a register ID file (see the TAG generated by RRC 204 in col.9, lines 9- 46, see the RRC 204 for facilitating the hazard detection in col.7, lines 5-24).

9. As to the remarks (argument D) regarding Wang by applicant on 07/22/05, Wang did not expressly show the aliasing of the rows of register files, see paragraph 7 above.

10. Claims 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iadonato et al. (5,371,684) in view of Clift (6,598,149).

11. As to claim 7, Iadonato also included at least :

a) a register file (1 17 register file) (see fig.II;

b) register ID file (it is ID file because it compared the addresses of the registers) for providing hazard detections (see fig.2 108) by common detection logic (see how the conflict of the source and destination registers being detected in col.6, lines 63-68, col.7, lines 1-20) .

12. Iadonato did not disclose the row to row hazard detection as claimed. Iadonato disclosed register hazard detection in row to column format (see figs. 2). However, Clift disclosed a system including register file (10) of R0-R7 architectural registers, each of the R0-R7 occupied one row in the register file (10) (see fig.1). It would have been obvious to one of ordinary skill in the art to use Clift in Iadonato for including the row to row detection as claimed because the use of Clift could provide the control ability of Iadonato to accept specific group of registers in rows in an integrated format, thereby

eliminating the circuit overheads of the memory, and therefore, reducing the wait time caused by the hardware, and it could be done by configuring the register file of Clift, which taught the architectural registers were organized in rows, into Iadonato with modified read/write pod, such that the particular row of the register file of Clift could be recognized by Iadonato in order to enhance the hazard detection capability of Iadonato, and in doing so, provided a motivation.

13. As to applicant's remark (argument c) on 07/22/05, applicant argued that in claim 7 when register file ID aliases two or more registers of the register file. When the data hazard detection logic compares a first register ID to a second register ID, it effectively compares two or more rows of the register file (aliased by the first register ID) to two or more rows of the register file (aliased by the second register ID), and the register identifier for one row of the register file, data hazard detection logic does not distinguish between any of the aliased rows within the register file when comparing row-to-row. Applicant is reminded that unclaimed features cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)). For example, nowhere does applicant claim recite the comparison of the first register ID to a second register ID , and the comparison of the two or more rows of the register file to two or more rows of the register file.

14. Claims 13 , 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar (5,884,070) in view of Dye (5,706,478).

15. As to claim 13, Panwar also included :

a) aliasing at least one entry of the register ID file to two or more registers of the register file (see fig-I B, see [f4] and [f5] aliased with the f4 ID, see also the aliased registers for reducing dependencies in col.4, lines 20-24);

b) valuating matches between entries of the register ID files in the hazard detection logic without distinguishing between common aliased entries of the register file (see no distinguishing of the common aliased entries in fig.1B, both addresses referring to the same datum in col.2, lines 50-57, see the dependencies detection in col.3, lines 25- 67, col.4, lines 1-19, col.8, lines 17-54).

16. Panwar did not show register file size as claimed. However, Dye disclosed a system including a register file comprising 128 registers (e.g. see col.7, lines 47-50 (205)). It would have been obvious to one of ordinary skill in the ad to use Dye in Panwar for selecting a 128-register register file as claimed because the use of Dye could provide Panwar the capability to adapt to a greater number of the storage capacity , and because Panwar was also directed to the processing of numeric precision method, which was a suggestion of the need for including larger size of registers in order to accept the numerical result in greater bandwidth, and for doing so, provided a motivation.

17. As to claim 14, see the fewer possible dependencies in col.8, lines49-54, col.10, lines 34-37, see also the aliased registers for reducing dependencies in col.4, lines 20-24). The fewer the dependencies , the less the hazard detection logic is needed.

18. As to remarks (argument B) by applicant on 07/22/05 that Dye did not disclose data hazard detection logic and the aliasing, Dye was used to supplement the teaching of register file size (col.7, lines 47-50 [205]). The reasons of obviousness ahs already been discussed in paragraph 16 above, therefore, it will not be repeated herein.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

19. Claims 8-12, 15, 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Panwar (5,884,070).

20. As to claim 8, Panwar taught:

a) aliasing each register identifier of a group of register identifiers to two or more registers (see the aliased registers in fig.1 B);

b) determining data hazard within the register file by presenting one or more register identifiers (see the determination of data dependencies in col.3, lines 39-67, col.4, lines 1 - 1 9).

21. As to claim 9, Panwar also mapped non-overlapping registers (see f4 and f6 in fig.1B)

22. As to claim 10, Panwar also included two more rows in hazard detection logic (see dependencies detection in col.3, lines 39-67, col.4, lines 1-19).

23. As to 11, see the fewer possible dependencies in col.8, lines 49-54, col.10, lines 34-37).

24. As to claim 12, Panwar also taught 32 register identifiers (see fig.1A f0-f31).

25. As to claim 15, Panwar taught :

a) aliasing each register ID within hazard detection logic to tow or more registers of a register file (see fig.1B)',

b) determining the data hazard by matching register ID within the detection (see the dependencies detection in col.3, lines 25-67, co1.4, lines 1-19, col.8, lines 17-54).

26. As to claim 16, Panwar disclosed (see also aliased registers and the reduction of dependencies in col.3, lines 49-67, col.4, lines 1-23 of Panwar for background teaching of aliasing):

a) aliasing two groups of registers (see odd group and even group in fig.1B) of a register file to one group of register ID (the register ID column in fig.1B);

b) detecting data hazard associated with the first the first aliased register ID to second aliased ID within the hazard detection (see dependencies detection identified by operand identifiers and the possible and second register by comparing dependencies in aliased f4 and f5 registers in col.3, lines 25-67, col.4, lines 1-19, col.8, lines 1 7-54).,

wherein each register ID (see f4 ID) aliased to one register of each of the register groups (see odd and even registers, both f4 and f5 aliased to f4 register ID), the two groups of registers overlapped in hazard detection logic (see fig.1B).

27. As to the overlap of register groups, examiner believes that it is important to understand how the registers were aliased in Panwar. Panwar's registers [f4] is a 64 bit long (see col.2, line 60) , and register [f5] is 32 bit long (see col.2, lines 63-64), therefore, register [f5] overlapped with the lower portion of register [f4]. Therefore, the even registers (one group) are overlapped with odd registers (second group).

28. As to the remark filed in the Appeal Brief, applicant had argued that applicant's aliases addresses do not refer to the same datum, and consecutive registers are not aliased. However, applicant is reminded that unclaimed features cannot be used to overcome the prior art (e.g. see CCPA In re Lundenberg & Zuschlag, 113, USPQ 530, 534 (1957)). For example, nowhere does applicant claim recite that aliased addresses do not refer to the same datum, and consecutive registers are not aliased, or the like. For example, no recitation of aliased addresses with the data , nor the relation of consecutive registers can be found in the claim.

29. Claim 16 reciting the overlapping of two more groups of registers (last 2 lines) while claim 1 reciting the overlap of first and second register identifiers (last 2 lines). Panwar did teach the overlapping of two groups of registers (see discussions set forth

in paragraph 11). Therefore, claim 16 is rejected by Panwar. The reasons for allowance of claim 1 is set forth in next paragraph.

30. Claims 1-3 are allowable over the art of record for reciting the combined features of identifying a first group of registers within a register file, aliasing the first group of registers to first register identifiers, the detection of data hazards associated with the first register identifiers, identifying a second group of registers within the register file, the aliasing of the second group of registers to second register identifiers, and the data hazards detection associated with the second register identifiers , the first and second register identifiers overlap in hazard detect logic across two or more rows of the register file.

31. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the mapping of the sequential 32 -registers with common hazard logic to more than 32 stacked registers of the register file to alias in 32-register sequences.

32. The prior art made of record and not relied upon is considered pertinent to

33. applicant's disclosure. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Orenstein et al. (5,835,748) is cited for the teaching of aliasing two register groups (see fig.3A, col.9, lines 7-24, col.10, lines 1-42).

Panwar (5,884,070) , Dye (5,706,478) , Iadonato et al. (5,371,684) , Clift (6,598,149), and Wang et al. (5,826,055) were cited one the record , therefore, copies are not included herein.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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